Programme Objective:

Design and implementation methodology of :

1) Analog front end for sensor interface: Instrumentation Amplifier (IA), chopper, Variable Gain Amplifier (VGA).
2) Data converters: SAR & pipelined ADC.
3) Digital VLSI: a) Static MOS gate circuits b) High-Speed CMOS Logic Design c) Transfer Gate and Dynamic Logic Design) VLSI architectures for video processing.
4) RF circuits: Introduction to RFIC design.
5) Design and implementation of typical RF Tx-Rx sub-components:(a) Low Noise Amplifier (LNA) (b) Mixer c) Frequency synthesizer (d) Power amplifier (e) Lay out and chip level integration.

Design Methodology:

From pen-paper design of various mixed signal/RF circuit blocks to schematic level implementation and then sub-sequent physical design, post-layout synthesis and simulation.

Eligibility:

1) He/she must be a faculty member in the Department of Electronics and Communication Engineering / Electrical Engineering / Computer Science and Engineering / Instrumentation Engineering / Information Technology / Physics with basic VLSI knowledge / Mathematics with basic VLSI knowledge / Material Science with basic VLSI knowledge / related Departments and Centres.
2) B.E./B.Tech. or equivalent degree holders in the above mentioned disciplines with minimum teaching experience of 2 years and moderate teaching experience in the area of Analog and Digital Circuits.
3) M.E./M.Tech. degree holders in the above mentioned disciplines with minimum teaching experience of 1 year and moderate teaching experience in the area of Analog and Digital Circuits.
4) Ph.D. degree holders should have a minimum teaching experience of 1 year and moderate teaching experience in the area of Analog and Digital Circuits.

Patron:

Hon. Mr. Samir Bhujbal,
Trustee, Mumbai Educational Trust.

Convener:

Dr. V.P.Wani,
Principal, MET's Institute of Engineering, Nashik

Workshop Coordinator:

Prof. Rajesh Rehpade (M: 98222 02099)
Email: rehpaderajesh@gmail.com

Remote Centre Coordinator:

Mrs. Manjusha Khond (M: 99226 26582)
Email : manjushak_ioe@bkc.met.edu

How to Apply:

Those wishing to attend this course should first register online at www.**nmeict.iitkgp**.ernet.in. Enrollment is strictly online, and no other mode of application will be entertained.

Fees:

This ISTE STTP on **'CMOS, Mixed Signal and Radio Frequency VLSI Design'** is funded by the National Mission on Education through ICT (MHRD, Government of India), therefore **there is no course fee** for participation.

Accommodation for outstation Participants:

Remote Center will provide tea/lunch on each day of the workshop, and accommodation to limited number of outstation participants. **Travel expenses up to Rs. 1000/- one way and one-time will be reimbursed against proof of actual expenditure, for participants beyond a distance of 100 Km.**

For more details contact:

Mr. Shekhar Shinde
Department of E & TC Engineering,
MET's Institute of Engineering,
Bhujbal Knowledge City,
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Mobile: 98224 25220.
Email: shekharshinde100@gmail.com

TWO WEEK ISTE

SHORT TERM TRAINING PROGRAMME ON

CMOS, MIXED SIGNAL AND RADIO FREQUENCY VLSI DESIGN

Physical participation at Remote centers during

30th January 2017 to 4th February, 2017

Conducted by

Indian Institute of Technology, Kharagpur

Under NMEICT, MHRD, New Delhi

Organized by

Department of
E & TC + Electronics Engineering,
MET's Institute of Engineering,
Bhujbal Knowledge City,
Adgaon, Nashik – 422 003.

Tel.: (0253) 2303515 | Telefax: (0253) 2303203
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MET Bhujbal Knowledge City

About the Institute:

MET's Institute of Engineering, under the umbrella of Bhujbal Knowledge City, is running six UG programs in Mechanical, Civil, Electrical, Computer, Information Technology and Electronics & Telecommunication and P G programs – M.E. (CAD Manufacturing & Engineering), M.E. (Computer Engineering) and MCA. It is also a recognized research centre for Doctorate programs in Mechanical and Computer Engineering. All the programs are approved by AICTE, DTE and affiliated with Savitribai Phule Pune University, Pune.

About the Department:

The departments of Electronics and E&TC Engineering were established in the year 2006 with the inception of MET's Institute of Engineering, Bhujbal Knowledge City, with intake of 60 each.

We are having highly qualified and dedicated staff members with variety of academic as well as industrial experience.

Departments are equipped with 14 state of the art laboratories such as Hi Tech PCB lab with PTH setup, Process control, DSP, VLSI, Embedded lab etc.

The aim of the department is to produce quality engineering professionals in the field of Electronics and Communication.

The Departments has close interaction with industry and the students are exposed to the industrial world. The Training & Placement Cell, Alumni Association and Students' Association are the strong organs of the Departments. The students have been placed in various reputed companies like TCS, Bosch, Siemens, Syntel, Zensar, Rishabh Instruments, Indian Army etc.

Salient Features of the Department

- A good combination of faculty with academic & industrial experience.
- Highly qualified and dedicated staff members.
- Faculty members have contributed to the research publications at national and international conferences.

Course Content:

1. **Radio Frequency Integrated Circuits (RFIC) :**

- **Module-A** Fundamental of RFIC design, How RF design alters from traditional analog design. Various commercial protocols, basic Tx-Rx Architecture.
- **Module-B** Various performance parameters, Noise.
- **Module-C** Design of LNA, VCO, Mixer and frequency synthesizer, Power amplifier, High speed I/O (SERDES), layout of RF circuit design.

2. **Mixed Signal Blocks :**

- Digital VLSI Design:High-Speed CMOS Logic, Transfer Gate and Dynamic Logic
  a) Basics of video processing
  b) VLSI Architectures for video processing
- Analog Design: Analog front-end electronics (AFE), SAR ADC, Pipelined ADC.

Teaching Faculty:

- **Prof. T. K. Bhattacharya,** Department of Electronics & Electrical Communication Engineering. IIT Kharagpur,
  email: tkb@ece.iitkgp.ernet.in
- **Prof. Indrajit Chakrabarti,** Department of Electronics & Electrical Communication Engineering. IIT Kharagpur,
  email: indrajit@ece.iitkgp.ernet.in
- **Dr. Mrigank Sharad,** Department of Electronics & Electrical Communication Engineering. IIT Kharagpur,
  email: mrigank@ece.iitkgp.ernet.in

Important Dates:

- Last date for online registration: 28th Nov., 2016
- Face-to-face workshop: 30 Jan. to 4 Feb., 2017

Note: Seats are limited to 30 **participants** only, to be filled on first come first serve basis.

Who may benefit:

The workshop is likely to benefit regular/visiting faculty colleagues who are teaching subjects like VLSI Design, Fundamentals of Radio Frequency Engineering, Design and Implementation of Mixed Signal Circuits and Systems, Design and Analysis of Radio Frequency Integrated Circuits, Mixed Signal and RFIC Design, Analog Front-End Design, Digital VLSI Circuits, VLSI Architecture for Video Processing etc.

STTP format

1. The participating teachers will complete the equivalent of two-week full time work online, spread over 6 physical weeks where video lectures and assignments will be uploaded beforehand.
2. After completing the online assignments spread over 4 to 5 weeks the participants will assemble at the selected Remote Centers for 6 days face to face interaction and lecture sessions through A-VIEW and will complete team assignments, tutorials, quizzes etc.
3. Offline assignments will be uploaded and the participants will have to complete these assignments within a stipulated time.
4. There will also be a system of students' feedback in the Main STTP.

Course domain:
Electronics Engineering / Electrical Engineering / Computer Science and Engineering

Expectation from the participants:
It is assumed that before taking the courses, the participants are familiar with introduction to electronic circuit components, signal and system theory, VLSI design technology and basic CAD flow for electronic system.